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APPLICATION

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TITLE: LOCK-IN PINNED PHOTODIODE PHOTO-DETECTOR

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LOCK IN PINNED PHOTODIODE PHOTODETECTOR

Cross Reference To Related Applications

This application is a continuation of U.S. Patent Application No. 09/378,565, filed August 19, 1999 (allowed), which claims the benefit of the U.S. Provisional Application No. 60/097,135, filed on August 19, 1998, which is incorporated herein by reference.

Background

Certain applications require measuring aspects that are based on the speed of light.

For example, range finding can be carried out using optics. An optical signal is sent. The reflection therefrom is received. The time that it takes to receive the reflection of the optical signal gives an indication of the distance.

The so called lock-in technique uses an encoded temporal pattern as a signal reference. The device locks into the received signal to find the time of receipt. However, noise can mask the temporal pattern.

A lock in photodetector based on charged coupled devices or CCDs has been described in Miagawa and Kanada "CCD based range finding sensor" IEEE Transactions on Electronic Devices, volume 44 pages 1648-1652 1997.

CCDs are well known to have relatively large power

consumption.

Summary

The present application describes a special kind of lock in detector formed using CMOS technology. More specifically, a lock in detector is formed from a pinned photodiode. The photodiode is modified to enable faster operation.

It is advantageous to obtain as much readout as possible to maximize the signal to noise ratio. The pinned photodiode provides virtually complete charge transfer readout.

Fast separation of the photo-generated carriers is obtained by separating the diode into smaller sub-parts and summing the output values of the subparts to obtain an increased composite signal.

Brief Description of the Drawings

These an other aspects will now be described in detail with reference to the accompanying drawings, wherein:

Figure 1 shows a basic block diagram of the system;

Figure 2 shows a block diagram of the multiple photodiode parts;

Figure 3 shows a block diagram of the system as used in range finding;

Figure 4a and 4b show pixel layouts; and

Figure 5 shows a cross section of the pinned photodiode.

Description of the Preferred Embodiment

The present application uses a special, multiple output port pinned photodiode as the lock in pixel element. The photodiode is preferably part of a CMOS active pixel image sensor, of the type described in US patent no 5,471,505. Hence, the system preferably includes in-pixel buffer transistors and selection transistors, in addition to the CMOS photodetector.

Figure 1 shows a pinned photodiode with four output ports, labeled as out1-out4. Each of the output ports is used to receive a reflection for a specified time duration. Each output becomes a "bin". The counting of the amount of information in the bins enables determination of the reflection time, and hence the range.

Pinned photodiodes are well known in the art and described in U.S. Patent No. 5,904,493. A pinned photodiode is also known as a hole accumulation diode or HAD, or a virtual phase diode or VP diode. Advantages of these devices are well known in the art. They have small dark current due to suppression of surface generation. They have good quantum efficiency since there are few or no polysilicon gates over the photosensitive region.

Pinned photodiodes can also be made into smaller pixels because they have fewer gates.

The basic structure of the pinned photodiode lock in pixel is shown in Figure 1. Four switched integrators are formed respectively at four output ports. Each gate is enabled during a specified period. The different integrators integrate carriers accumulated during the different periods. The first integrator accumulates carriers between 0 and $\pi/2$, the second between $\pi/2$ and π, the third between π and $3\pi/2$ and the fourth between $3\pi/2$ and 2π time slots.

Assuming the light to be a cosine phase, then the phase shift of the detected light is given by

$$\mathit{arctan}[(L1-L3)/(L2-L4)],$$

where L1, L2, L3 and L4 are the amplititudes of the samples from the respective first, second, third and fourth integrators. These four phases are obtained from the four outputs of the photodiode.

The first pinned photodiode 100 is connected to an output drain 102 via gate 1, element 104. This receives the charge for the first bin. Similarly, gates 2, 3 and 4 are turned on to integrate/bin from the second, third and fourth periods.

It is important to obtain as much signal as possible from the photodiode. This can be done by using a large photodiode.

However, it can take the electrons a relatively long time to escape from a large photodetector.

The present system divides the one larger photodiode into a number of smaller diodes, each with multiple output ports. Figure 2 shows the system.

A number of subpixels are formed. Each includes a number of pinned photodiodes 200, each with four ports. Each of the corresponding ports are connected together in a way that allows summing the outputs of the photodiodes. For example, all the gate 1 control lines are connected together as shown. The outputs from all the port 1s are also summed, and output as a simple composite output. Similarly, ports 2, 3 and 4's are all summed.

Figure 3 shows the circuit and driving waveforms for the system when used as a range finder. A pulse generator drives selection of the active output. Each time period is separately accumulated, and output. If a 40 MHZ pulse generator is used, 25 ns resolution can be obtained.

Figure 4A and 4B show representative pixel layouts. Figure 4A shows a 6 by 6 square micron pixel layout while Figure 4B shows an 8½ by 8½ micron pixel layout. In both Figures, four outputs are shown.

Figure 5 shows a cross sectional potential diagram of an exemplary pinned photodiode.

Assuming the operation frequency of modulated light is 10 megahertz with a 25 nanosecond integration slot, the generator carrier has a time of flight within this limit. This resolution time constrains the size of the detector. In addition, the characteristic diffusion time in a semiconductor device is L^2/D, where D is the diffusion coefficient. This time originates from the continuity equation and the diffusion equation, and defines how soon the steady state will be established in the area of size L. Hence, for a 10 cm square per second electron diffusion coefficient, the characteristic size of the pinned photodiode could be less than 5 microns.

Other embodiments are also contemplated to exist within this disclosure. For example, other numbers of output ports, e.g. 2-8, are possible. While this application describes using a pinned photodiode, similar operations could be carried out with other CMOS photodetectors, e.g., photodiodes and photogates.

Such modifications are intended to be encompassed within the following claims.